A New Six-Switch Five-Level Active Neutral Point Clamped Inverter for PV Applications

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***Abstract*—Multilevel inverters are one of the preferred solutions for medium-voltage and high-power applications and have found successful industrial applications. Five-level active neutral point clamped inverter (5L-ANPC) is one of the most popular topologies among five-level inverters. A six-switch 5L-ANPC (6S-5L-ANPC) topology is proposed. Compared to the conventional 5L-ANPC inverters, the 6S-5L-ANPC reduces two active switches and has lower conduction loss. The proposed modulation enables the 6S-5L-ANPC inverter to operate under both active and reactive power conditions. The flying-capacitor capacitance is designed under both active and reactive power conditions. The analysis shows the proposed topology is suitable for photovoltaic grid-connected applications. A 1 KVA single-phase experimental prototype is built to verify the validity and flexibility of the proposed topology and modulation method.**

***Index Terms*—Active neutral point clamped (ANPC), flying-capacitor (FC), multilevel inverter, pulse width modulation (PWM).**

I. Introduction

MULTILEVEL inverters have received increased attention in both academia and industry nowadays as one of the optimal solutions of power conversion for medium- and high-power applications [1]–[4]. For medium-power application, the motivation for the use of multilevel inverters is to reduce the switch voltage stress as well as the output filter size. They also have the advantages of improved output quality, lower total harmonic distortion (THD), lower common-mode voltage, and lower electromagnetic interference in contrast to their two-level counterparts [5]. Furthermore, the multilevel inverters have possibility to achieve higher efficiency over the conventional inverters due to the use of low-voltage drop devices, leading to their low-voltage application such as photovoltaic (PV) cells [6]–[8].

There are three types of classic multilevel inverter topologies: neutral point clamped (NPC) type [9], [10], flying-capacitor (FC) type [11], [12], and cascaded H-bridge (CHB) type [13], [14]. A single-phase leg of three types of topologies generating five-level output are shown in Fig. 1.

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The NPC-type multilevel inverters generate the voltage levels from the neutral point voltage by adopting the clamping diodes. However, when voltage levels increase, more clamping diodes, active semiconductor switches, and dc-link capacitors are needed. Excessive number of clamping diodes is connected in series to block the higher voltage, thus producing more conduction losses and generating reverse recovery currents that affect the switching losses of other devices. The dc-link voltage balancing problem is another issue for higher levels NPC inverters.

As another type of classic multilevel inverters, the FC inverter produces the required output voltage levels by summing the FC- and dc-link voltages. The increased number of capacitors in higher levels leads to complex control method to balance the voltages of both dc-link capacitors and FCs. The higher switching frequency to keep the capacitors properly balanced and capacitors maintenance costs result in the less industrial penetration of FC type.

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. Similarly, to have more output levels, more cells are needed. This will lead to impracticality of this type of topology since more isolated dc sources are required.

A generalized multilevel inverter topology is presented in [15], which is capable of balancing each voltage level regardless of the inverter control and load characteristics. The aforementioned conventional multilevel inverters can be derived from this generalized inverter topology. Besides, some new multilevel topologies, such as multilevel modular capacitor clamped [16] and zigzag multilevel inverter [17] can also be derived using the method in [15].

Hybrid multilevel inverters topologies combine some features of NPC and FC that provides the possibilities to take advantages of both topologies [18], [19]. Among hybrid topologies, the five-level active NPC (5L-ANPC) inverter provides an acceptable compromise between cost and performance [20]–[28]. As shown in Fig. 2(a), the 5L-ANPC inverter combines a 3L-ANPC leg with a 3L-FC power cell. The number of levels is increased with the levels introduced by the FC. This topology enables the modularity factor that is lacking in the NPC-type inverter by adding the FC to reach higher level without adding series-connected diodes. In addition, the ANPC inverters splits the dc-link into two capacitors, so the complexity of dc-link capacitor voltages balancing is reduced compared to the conventional NPC- and FC-type inverters which need four dc capacitors in

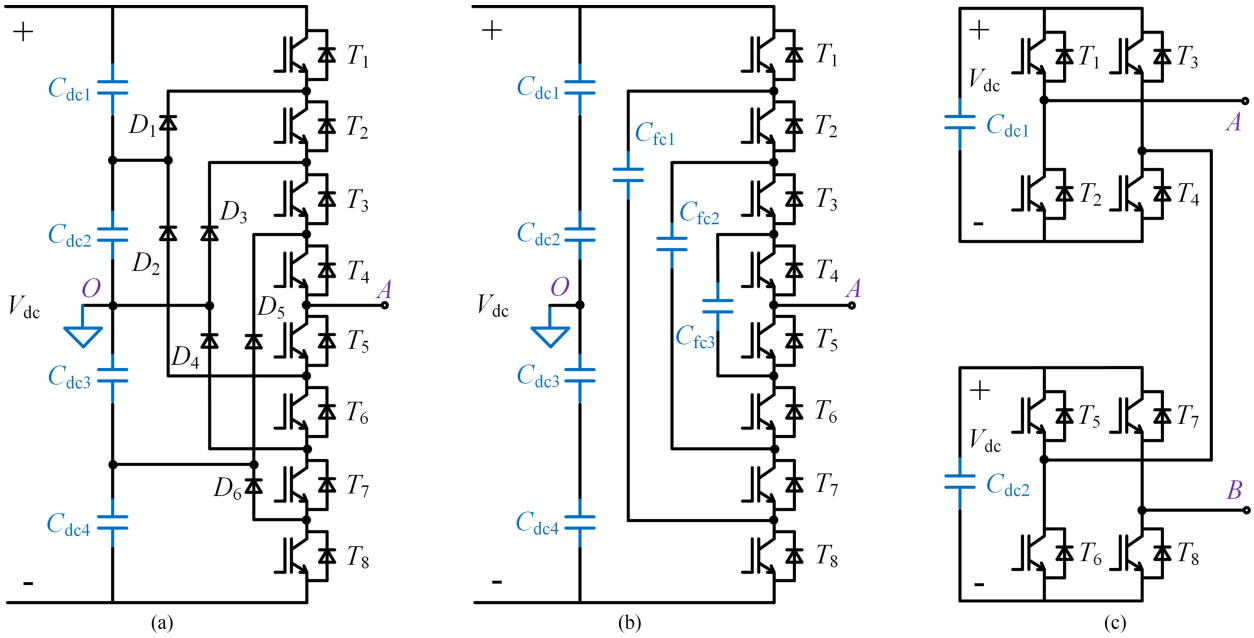

Fig. 1. Conventional multilevel inverter topologies (five-level). (a) NPC type. (b) FC type. (c) CHB type.

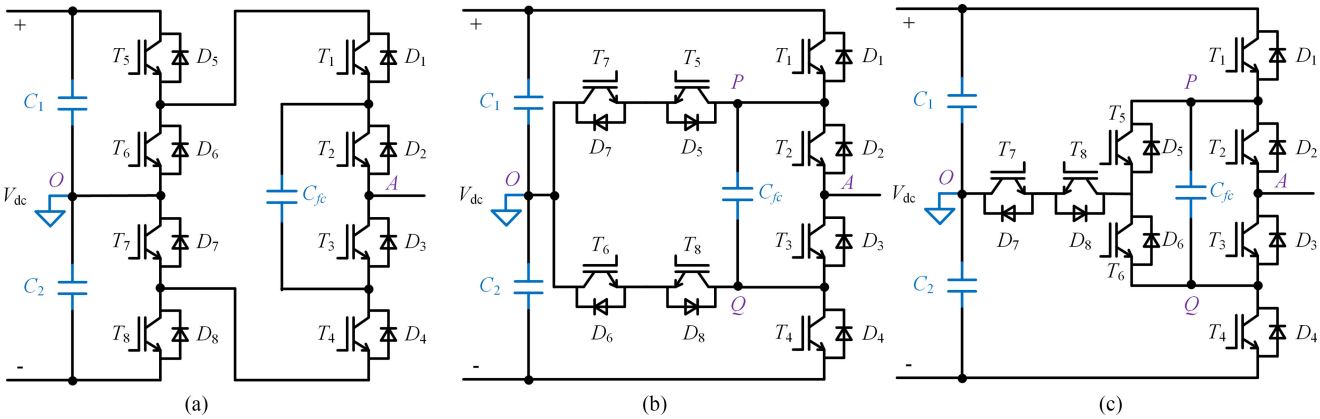

Fig. 2. Conventional 5L-ANPC inverter topologies. (a) Type I. (b) Type II. (c) Type III.

series. Due to the reduced costs, volume, and control complexity, the 5L-ANPC inverter is receiving more attention recently and is already commercially used for medium power level industrial applications [29]. Fig. 2(b) and (c) shows additional two types of 5L-ANPC inverter [30].

The redundant switching states in ANPC inverters allow the voltage across FC to be regulated. To generate the switching pulses and simultaneously regulate the FC voltage, a variety of modulation strategies have been presented such as carrier-based pulse width modulation (PWM) [31], modified carrier-based PWM [23], real-time THD minimization [32], and selective harmonic elimination PWM [33], [34].

From Fig. 2, it is observed that for the existing conventional 5L-ANPC inverter topologies, at least eight active switches are required. And from the point view of industrial application, it would be more desirable if the cost of the system can be reduced. The motivation of this paper is to reduce the number of active switches. For PV application, the output current and grid voltage are generally in phase, so some of reactive current paths can be removed. Based on this, a novel six-switch five-level ANPC (6S-5L-ANPC) inverter topology is proposed [35]. Compared to the conventional 5L-ANPC inverter, the proposed topology requires only six active semiconductor switches, reducing the volume of system. Additionally, with the proposed modulation method applied to the proposed 6S-5L-ANPC inverter, the system is capable of operating under both active and reactive power conditions.

This paper is organized as follows: Section II describes operating principles of the proposed 6S-5L-ANPC inverter; Section III makes a comparison between the conventional 5L-ANPC and 6S-5L-ANPC inverters in terms of device voltage stress, efficiency and system volume; Section IV discusses the modulation strategy of 6S-5L-ANPC topology; Section V provides a design method for the FC capacitance under active and reactive power conditions; Section VI gives the simulation verification and the maximum

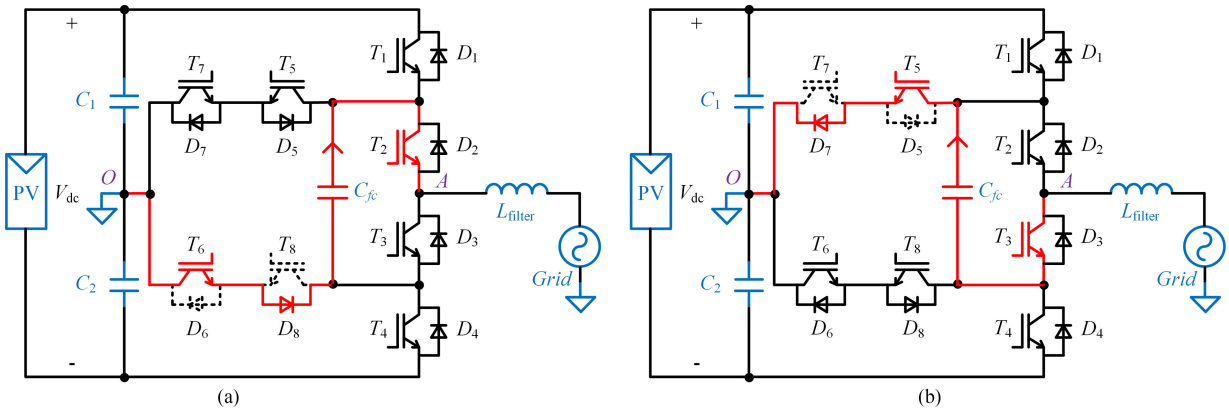

Fig. 3. Active current paths for two switching states of type II conventional 5L-ANPC inverter. (a) +1 level switching state. (b) –1 level switching state.

reactive power capability of the proposed topology; Section VII presents the experimental results; and Section VIII gives the conclusion.

II. Operating Principles of the Proposed 6S-5L-ANPC Inverter

A. Introduction of the 6S-5L-ANPC Inverter

The 5L-ANPC inverter is a good choice for renewable energy harvesting because of its improved efficiency and output waveform. The configuration of Type II conventional 5L-ANPC inverter is shown in Fig. 2(b). First, the dc-link voltage is defined as $V_{\rm dc}$. The dc-link consists of two capacitors (C_1, C_2), whose voltages are rated at half of dc voltage ($V_{\rm dc}/2$). An FC ($C_{\rm fc}$) is required to provide one quarter of dc voltage ($V_{\rm dc}/4$). Five output voltage levels $+V_{\rm dc}/2$, $+V_{\rm dc}/4$, 0, $-V_{\rm dc}/4$, and $-V_{\rm dc}/2$ (which are defined as +2, +1, 0, –1, and –2, respectively) are achieved by summing the FC voltage and dc-link capacitor voltages.

For PV grid-connection application, the inverter output current is required to be in phase with grid voltage. In this situation, some of the reactive current paths can be ignored, which means some active switches can be replaced by fast recovery diodes. For the switching states which output +2 and –2 levels, (T_1, T_2) and (T_3, T_4) are turned ON for active current flow and the reactive current path is pass through their anti-parallel diodes. So, these four active switches cannot be removed. Similarly, for the switching states which output +1 and –1 levels, (T_1/D_1, T_3/D_3) and (T_2/D_2, T_4/D_4) are turned ON. Both switching states are charging the FC in unity power factor condition. To balance the FC voltage, there are additional two switching state which also output +1 and –1 level to discharge the FC, which are called redundant switching states, as shown in Fig. 3(a) and (b). The red line shows the active power current path. With above motivation, the parts for reactive power operation (dashed parts) can be ignored. There are also two redundant 0 switching states: one is through T_6, D_8, and T_2; the other is through T_3, T_5, and D_7. Since T_1/D_1 to T_4/D_4 are kept, there is no change for 0 output level switching states. Finally, a novel 6S-5L-ANPC inverter topology is derived, as shown in Fig. 4.

In Fig. 4, six active power semiconductor switches (T_1–T_6) and two discrete diodes (D_7, D_8) are needed to generate five-level output. The outer switches (T_1–T_4) operate at switching frequency and inner switches (T_5, T_6) commutate at line frequency. Additionally, the current paths including T_5 and T_6 also flow through the fast recovery diodes, which can only achieve unidirectional current flow. Thus, the selection of inner switches (T_5, T_6) can be insulated-gate bipolar transistor (IGBT) without antiparallel diode, further reducing the system cost.

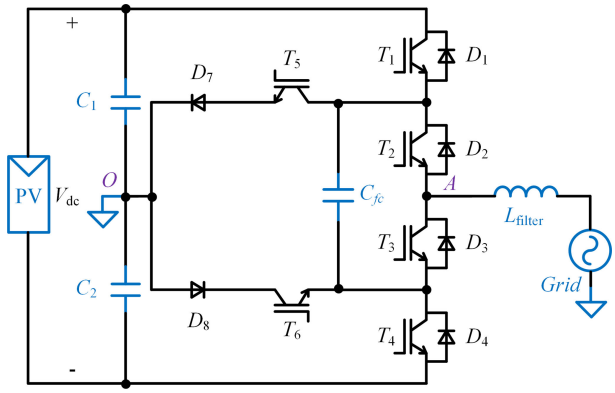

Fig. 4. Configuration of the proposed 6S-5L-ANPC inverter.

TABLE I
Switching States, Output Voltage, and Impact on the FC Voltage of 6S-5L-ANPC Inverter

	Active Switch State							Flying Capacitor $C_{\rm fc}$	
No	T_1	T_2	T_3	T_4	T_5	T_6	$V_{\rm out}$	$i_{\rm out} > 0$	$i_{\rm out} < 0$
A	1	1	0	0	0	1	+2	–	–
B	1	0	1	0	0	1	+1	Charge	Discharge
C	0	1	0	0	0	1	+1	Discharge	Charge
D	0	0	1	0	0	1	+0	–	–
E	0	1	0	0	1	0	–0	–	–
F	0	0	1	0	1	0	–1	Charge	Discharge
G	0	1	0	1	1	0	–1	Discharge	Charge
H	0	0	1	1	1	0	–2	–	–

As can be observed from Fig. 4, in contrast to the conventional 5L-ANPC inverters, which need eight active switches and other types of five-level inverters, which require more devices, the proposed 6S-5L-ANPC inverter employs only six active switches and two discrete diodes. The reduced number of active switches sacrifices some reactive current paths. However, with special

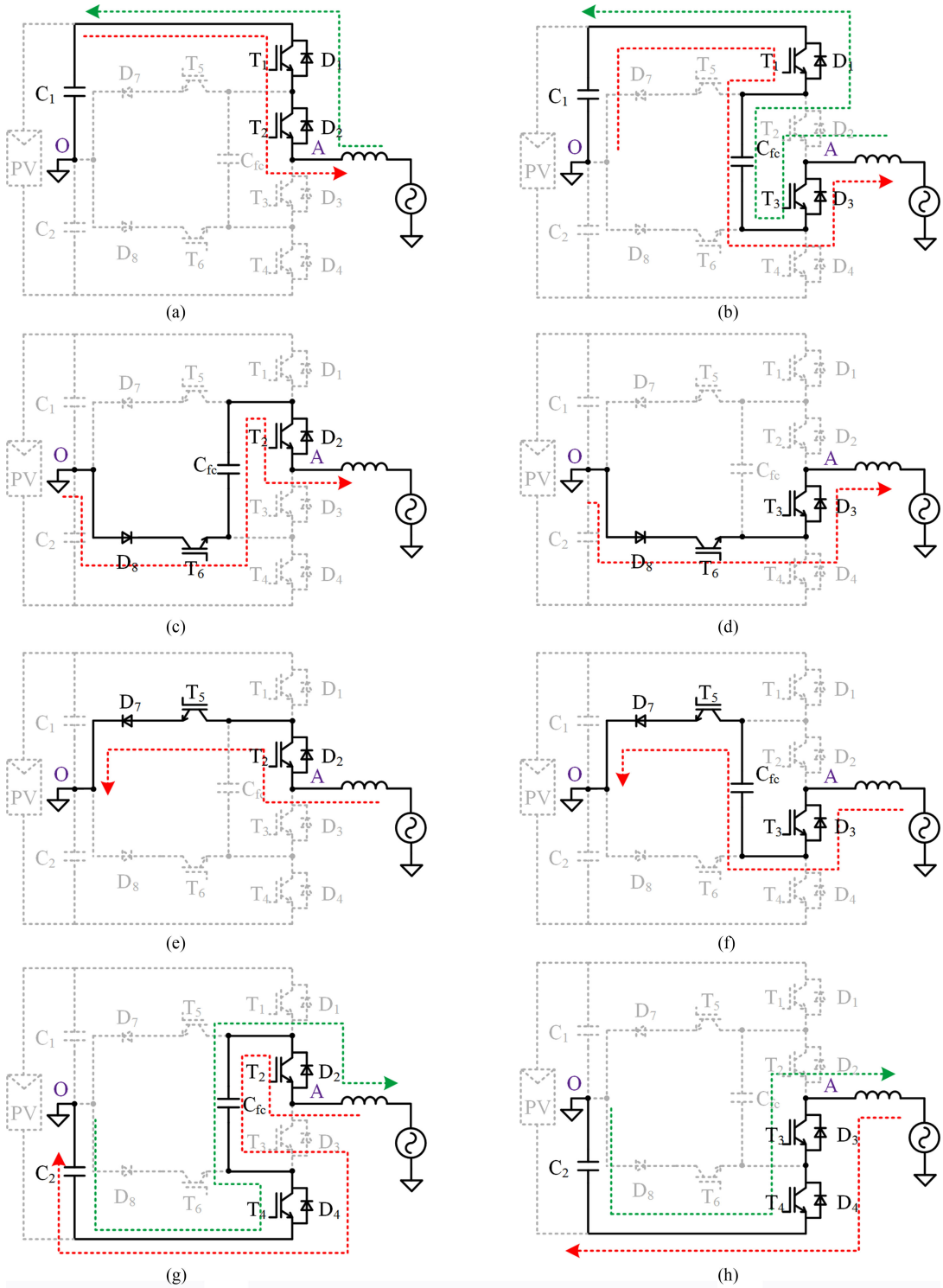

Fig. 5. Eight switching states for 6S-5L-ANPC inverter. (a) State A: +2. (b) State B: +1. (c) State C: +1. (d) State D: 0. (e) State E: 0. (f) State F: –1. (g) State G: –1. (h) State H: –2.

modulation method, the proposed topology has the capability of feeding reactive power into the grid to support the stability of the power system, which will be addressed in Section IV.

B. Operation of the 6S-5L-ANPC Topology

The 6S-5L-ANPC inverter consists of eight switching states that generate five-level voltage levels at the output based on capacitor voltages, as shown in Table I. The output current is defined as i_{out}. V_{out} represents the output voltage level. Fig. 5 shows eight different switching states (state A to H) and current paths (the red line shows the active current path while the green line represents the reactive power path).

In Table I, it is observed that there are three pairs of redundant switching states which generate same output voltage level: states

TABLE II
VOLTAGE STRESS AND SWITCHING FREQUENCY OF DEVICES FOR FOUR TYPES OF 5L-ANPC INVERTERS

	Type I 5L-ANPC		Type II 5L-ANPC		Type III 5L-ANPC		6S-5L-ANPC	
Device	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency
T_1/D_1	0.25 $V_{\rm DC}$	f_S	0.75 $V_{\rm DC}$	f_S for half line cycle	0.75 $V_{\rm DC}$	f_S for half line cycle	0.75 $V_{\rm DC}$	f_S for half line cycle
T_2/D_2	0.25 $V_{\rm DC}$	f_S	0.25 $V_{\rm DC}$	f_S	0.25 $V_{\rm DC}$	f_S	0.25 $V_{\rm DC}$	f_S
T_3/D_3	0.25 $V_{\rm DC}$	f_S	0.25 $V_{\rm DC}$	f_S	0.25 $V_{\rm DC}$	f_S	$V_{\rm DC}$	f_S
T_4/D_4	0.25 $V_{\rm DC}$	f_S	0.75 $V_{\rm DC}$	f_S for half line cycle	0.75 $V_{\rm DC}$	f_S for half line cycle	0.75 $V_{\rm DC}$	f_S for half line cycle
T_5	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$
T_6	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$
D_5	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	$f_{\rm Line}$	Not needed	Not needed
D_6	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	$f_{\rm Line}$	Not needed	Not needed
T_7	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle	Not needed	Not needed
T_8	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle	Not needed	Not needed
D_7	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle
D_8	0.5 $V_{\rm DC}$	$f_{\rm Line}$	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle	0.25 $V_{\rm DC}$	f_S for half line cycle

B and C are redundant switching states to generate $+1$ voltage level; similarly, (D, E) and (F, G) are redundant states to generate 0 and –1, respectively. Although the redundant states (B, C) and (F, G) generate the same output voltage level, their effect on the FC voltage is opposite to each other due to the change in the direction of the FC current. This leads to the possibility of regulating the FC voltage to a constant value ($V_{\rm dc}/4$). The sign of load current $i_{\rm out}$ and the deviation sign of FC voltage from its reference value are required to decide which redundant switching state is to be chosen.

In Fig. 5, it is observed that among eight switching states, four states (C, D, E, and F) allow unidirectional current flow due to the presence of discrete diode. Therefore, appropriate selection of switching states under reactive power operation is very important. The special modulation strategy for the proposed topology will be discussed in Section IV.

III. COMPARISON BETWEEN 6S-5L-ANPC AND THE CONVENTIONAL 5L-ANPC INVERTERS

To better illustrate the advantage of the proposed topology, it is important to make a comparison between the 6S-5L-ANPC inverter and the conventional 5L-ANPC inverters in terms of device voltage rating, switching frequency, efficiency, and system volume.

A. Device Voltage Stress and Switching Frequency

Table II shows the voltage stress and switching frequency of devices for four types of 5L-ANPC inverters. $f_{\rm Line}$ and f_S represent the line frequency and switching frequency, respectively.

Compared to the Type I 5L-ANPC inverter: the voltage stress of T_1/D_1 and T_4/D_4 for 6S-5L-ANPC inverters is increased to 0.75 $V_{\rm DC}$, which means a higher voltage rating device should be selected for these two switches. However, the switching loss of these two devices are generated in the same way as in the Type I 5L-ANPC inverter. For example, T_1/D_1 will carry the output current $i_{\rm out}$ when switched ON and block the voltage levels of 0.25 $V_{\rm DC}$ when switched OFF in the positive grid cycle. On the other hand, for Type I 5L-ANPC inverter, T_1/D_1 and T_4/D_4 are switched ON and OFF at high frequency f_S for the whole grid cycle; while for the proposed topology, T_1/D_1 and T_4/D_4 are only operating at high frequency for half line period and turned OFF for the other half line period, so the switching loss of these two devices will be lower (approximately half of the switching loss in Type I topology).

Compared to the Type II 5L-ANPC inverter: the voltage stress of devices in the proposed topology is the same as that of Type II 5L-ANPC topology, and two active switches are reduced.

Compared to the Type III 5L-ANPC inverter: the difference between the proposed topology and Type III is the voltage stress of T_5/D_5 and T_6/D_6 in Type III 5L-ANPC inverter is reduced to 0.25 $V_{\rm DC}$. However, the conduction loss of Type III 5L-ANPC topology is higher, which will be given in the following part.

B. Conduction Loss Analysis

The conduction loss comparison can be performed considering the number of connected devices in series when they are ON, as shown in Table III. The symbols $+$ and – represent the minimum and maximum number of conducting devices.

For Type I 5L-ANPC inverter, three devices are always connected in series to carry the main current for all eight states; while for the proposed topology, during the switching states A, B, G, and H, the output current is going through only two devices. Therefore, compared to the Type I 5L-ANPC topology, the conduction loss of the proposed topology during these four states is reduced by $1/3$, and the whole conduction loss is approximately reduced by $1/6$.

Compared to the Type II 5L-ANPC inverter: the conduction loss of the 6S-5L-ANPC inverter is the same as that of the Type II 5L-ANPC topology.

The difference between 6S-5L-ANPC and Type III 5L-ANPC topologies is: during the switching states C, D, E, and F, three devices are needed to conduct the output current for the 6S-5L-ANPC inverter, while Type III requires four devices. Similarly, compared to the Type III 5L-ANPC topology, the conduction loss of the proposed topology during four states C, D, E, and F is reduced by $1/4$, and the whole conduction loss is approximately reduced by $1/8$.

With the above analysis, it is concluded that the conduction loss of the proposed 6S-5L-ANPC topology is the same as that

TABLE III
CONDUCTION LOSS OF FOUR TYPES OF 5L-ANPC INVERTERS

Switching State		Type I 5L-ANPC		Type II 5L-ANPC		Type III 5L-ANPC		6S-5L-ANPC	
A (+2)	$i_{\rm out} > 0$	T_1, T_2, T_5	–	T_1, T_2	+	T_1, T_2	+	T_1, T_2	+
	$i_{\rm out} < 0$	D_1, D_2, D_5	–	D_1, D_2	+	D_1, D_2	+	D_1, D_2	+
B (+1)	$i_{\rm out} > 0$	T_1, T_5, D_3	–	T_1, D_3	+	T_1, D_3	+	T_1, D_3	+
	$i_{\rm out} < 0$	D_1, D_5, T_3	–	D_1, T_3	+	D_1, T_3	+	D_1, T_3	+
C (+1)	$i_{\rm out} > 0$	T_2, T_7, D_4	+	T_2, T_6, D_8	+	T_2, T_5, T_8, D_6	–	T_2, T_6, D_8	+
	$i_{\rm out} < 0$	D_2, D_7, T_4	+	D_2, D_6, T_8	+	D_2, D_5, D_8, T_6	–	Not needed	
D (0)	$i_{\rm out} > 0$	T_7, D_3, D_4	+	D_3, T_6, D_8	+	D_3, T_5, T_8, D_6	–	D_3, T_6, D_8	+
	$i_{\rm out} < 0$	D_7, T_3, T_4	+	T_3, D_6, T_8	+	T_3, D_5, D_8, T_6	–	Not needed	
E (0)	$i_{\rm out} > 0$	T_1, T_2, D_6	+	T_2, T_7, D_6	+	T_2, T_5, D_6, D_7	–	Not needed	
	$i_{\rm out} < 0$	D_1, D_2, T_6	+	D_2, D_7, T_5	+	D_2, D_5, T_6, T_7	–	D_2, T_5, D_7	+
F (–1)	$i_{\rm out} > 0$	T_1, D_3, D_6	+	D_3, T_7, D_5	+	D_3, T_5, D_6, D_7	–	Not needed	
	$i_{\rm out} < 0$	D_1, T_3, T_6	+	T_3, D_7, T_5	+	T_3, D_5, T_6, T_7	–	T_3, T_5, D_7	+
G (–1)	$i_{\rm out} > 0$	T_2, D_4, D_8	–	T_2, D_4	+	T_2, D_4	+	T_2, D_4	+
	$i_{\rm out} < 0$	D_2, T_4, T_8	–	D_2, T_4	+	D_2, T_4	+	D_2, T_4	+
H (–2)	$i_{\rm out} > 0$	D_3, D_4, D_8	–	D_3, D_4	+	D_3, D_4	+	D_3, D_4	+
	$i_{\rm out} < 0$	T_3, T_4, T_8	–	T_3, T_4	+	T_3, T_4	+	T_3, T_4	+

TABLE IV
SWITCHING LOSS OF FOUR 5L-ANPC INVERTERS

Switching State		Type I 5L-ANPC	Type II 5L-ANPC	Type III 5L-ANPC	6S-5L-ANPC	ΔV	ΔI
A (+2) ⟷ B (+1)	$i_{\rm out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
A (+2) ⟷ C (+1)	$i_{\rm out} > 0$	T_1, D_4	T_1, D_8	T_1, D_8	T_1, D_8	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_1, T_4	D_1, T_8	D_1, T_8	Not needed	0.25 $V_{\rm DC}$	$i_{\rm out}$
B (+1) ⟷ D (0)	$i_{\rm out} > 0$	T_1, D_4	T_1, D_8	T_1, D_8	T_1, D_8	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_1, T_4	D_1, T_8	D_1, T_8	Not needed	0.25 $V_{\rm DC}$	$i_{\rm out}$
C (+1) ⟷ D (0)	$i_{\rm out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
F (–1) ⟷ E (0)	$i_{\rm out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
G (–1) ⟷ E (0)	$i_{\rm out} > 0$	T_1, D_4	D_4, T_7	D_4, T_7	Not needed	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_1, T_4	T_4, D_7	T_4, D_7	T_4, D_7	0.25 $V_{\rm DC}$	$i_{\rm out}$
H (–2) ⟷ F (–1)	$i_{\rm out} > 0$	T_1, D_4	D_4, T_7	D_4, T_7	Not needed	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_1, T_4	T_4, D_7	T_4, D_7	T_4, D_7	0.25 $V_{\rm DC}$	$i_{\rm out}$
H (–2) ⟷ G (–1)	$i_{\rm out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	0.25 $V_{\rm DC}$	$i_{\rm out}$
	$i_{\rm out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	0.25 $V_{\rm DC}$	$i_{\rm out}$

of the Type II conventional 5L-ANPC topology, and is lower than Type I and Type III 5L-ANPC inverters.

C. Switching Loss Analysis

Table IV shows the switching loss in terms of switching states commutations.

Compared to the Type I 5L-ANPC inverter: as mentioned earlier, for 6S-5L-ANPC inverter, the devices T_1/D_1 and T_4/D_4 need to block 0.75 $V_{\rm DC}$ voltage when they are not conducting current. However, the switching loss of these two devices are generated in the same way as in the Type I 5L-ANPC inverter. From Table IV, it is observed that for all switching state transitions, the device voltage change is 0.25 $V_{\rm DC}$ and the current is output current $i_{\rm out}$. Therefore, if the device selection for 6S-5L-ANPC and Type I 5L-ANPC is the same, then the switching loss for two topologies should be identical. If higher voltage rating devices are selected for T_1/D_1 and T_4/D_4 in 6S-5L-ANPC topology, then its switching loss will be slightly higher than Type I due to the increased turn-ON energy for higher voltage rating device.

Compared to the Type II, III 5L-ANPC inverter: based on Tables II and IV, it is observed that, due to the same device selection and switching states commutations, the switching loss of the 6S-5L-ANPC inverter is the same as that of Type II and III 5L-ANPC inverters.

D. System Volume

In terms of the volume of dc-link capacitors: for all 5L-ANPC inverter topologies, including the proposed 6S-5L-ANPC inverter, the upper dc-link capacitor and FC are providing the energy to the output side in positive grid cycle, while during the negative grid cycle, the lower dc-link capacitor and FC are transferring the energy to the output side. Therefore, the dc-link capacitance selection for 6S-5L-ANPC is the same as the conventional 5L-ANPC inverters.

In terms of volume of FC: under unity power factor condition, the FC value of the proposed topology is the same as the conventional 5L-ANPC inverters. When the power factor is getting lower, with the same FC capacitance, the voltage ripple of the proposed topology will be larger than the conventional

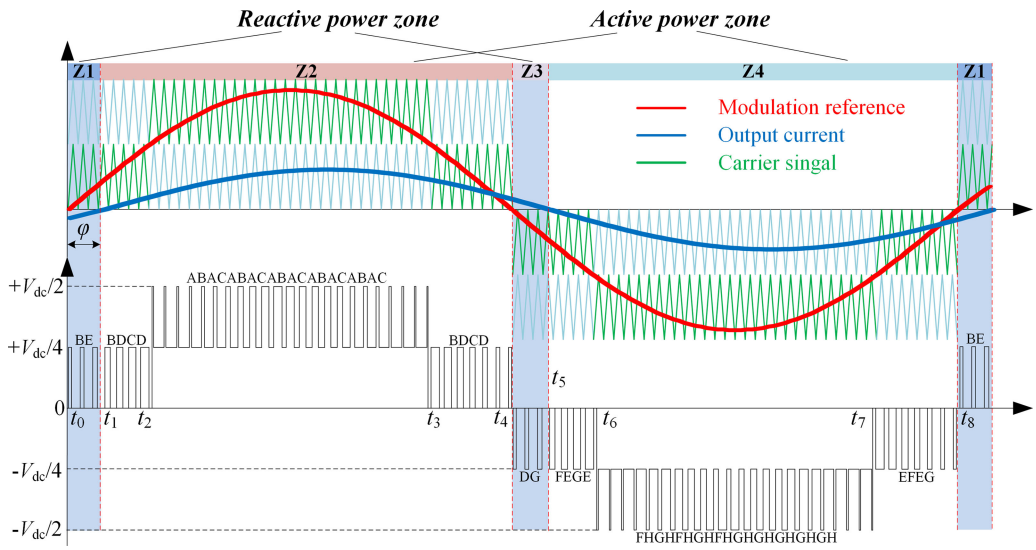

Fig. 6. PWM modulation for 6S-5L-ANPC inverter.

ANPC inverters. The specific analysis of FC design is discussed in Section V and the maximum reactive power capability of the proposed topology is presented in Section VI.

With the loss and cost analysis developed above, it is concluded that

1) the efficiency of the proposed topology is the same as the Type II 5L-ANPC inverter;
2) compared to the Type I 5L-ANPC topology, the conduction loss of the proposed topology is lower, but the switching loss of the proposed topology is slightly higher. Therefore, under high-power condition whose switching frequency is low, the proposed topology has higher efficiency over Type I 5L-ANPC inverter [30];
3) compared to the Type III 5L-ANPC inverter, the efficiency of the proposed 6S-5L-ANPC inverter is higher because its conduction loss is lower than that of the Type III 5L-ANPC topology;
4) the dc-link capacitance selection for 6S-5L-ANPC inverter is the same as the conventional 5L-ANPC inverters.

For high-power factor applications such as PV application, the proposed 6S-5L-ANPC topology is a good choice because it achieves the reduction of two active switches and the same performance as the conventional 5L-ANPC inverters.

IV. Modulation Strategy

As can be observed from Fig. 5, during the four switching states (C, D, E, and F), the current can only flow in one direction due to the use of fast recovery diode. Therefore, there are limitations for the selection of four switching states with unidirectional current path. This section describes the modulation strategy for the proposed 6S-5L-ANPC inverter.

The diagram of modulation for the 6S-5L-ANPC inverter under reactive power operation is shown in Fig. 6. The phase disposition PWM scheme is used because of its lower THD [36].

In Fig. 6, four carriers and one reference signals are used for one phase of the inverter. By comparing each of the carriers with the reference, the corresponding switching states are switched and five-level output voltage waveform is generated. From Fig. 6, it is observed that during a complete grid line cycle, four operating zones can be identified based on the polarities of the output current and grid voltage: in Z1 and Z3, the output current and reference voltage are in the opposite direction; in Z2 and Z4, the output current and reference voltage are in the same direction.

It is noted that both zero switching states (D and E) belong to unidirectional current path states. The selection of two redundant switching states which give zero output is based on the direction of the output current. So, from t_1 to t_5, the current is positive and mode D is chosen. Similarly, from t_0 to t_1 and t_5 to t_8, mode E is selected due to the negative output current.

Among two pairs of redundant states which output ± 1 level, states C $(+1)$ and F (-1) allow unidirectional current-flow path. These two states can only be used when the output voltage and current are in the same direction. Therefore, under a reactive power condition, when directions of current and voltage are different, only mode B $(+1)$ and G (-1) can be used to achieve 1 output level.

A. Modulation in Z1 [from t_0 to t_1]

During this period, the output voltage level varies between $+1$ and 0. In this region, only mode B can be used to generate $+1$ output because voltage and current are in the opposite direction. Therefore, the FC voltage cannot be regulated and it has always been discharged. For zero output, mode E is selected due to the negative current. So, the circuit rotates in the sequence of (B, E, B, E). The specific modulation in this region is shown in Fig. 7.

B. Modulation in Z2 [From t_1 to t_4]

From t_1 to t_2 and t_3 to t_4, the output voltage is also switched between $+1$ and 0. Both redundant $+1$ states (B, C) can be used, which gives an opportunity to regulate the voltage across FC. When actual FC voltage is lower than the reference value,

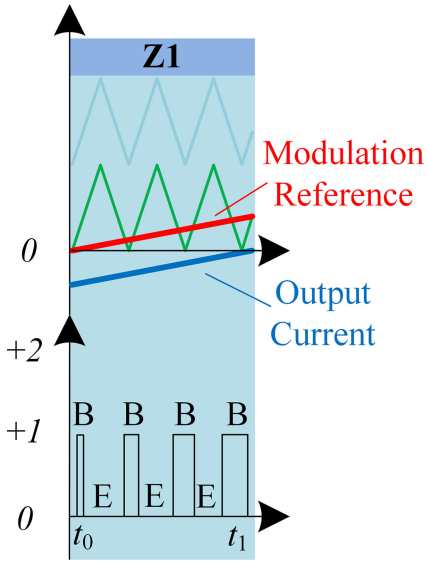

Fig. 7. PWM Modulation in Z1.

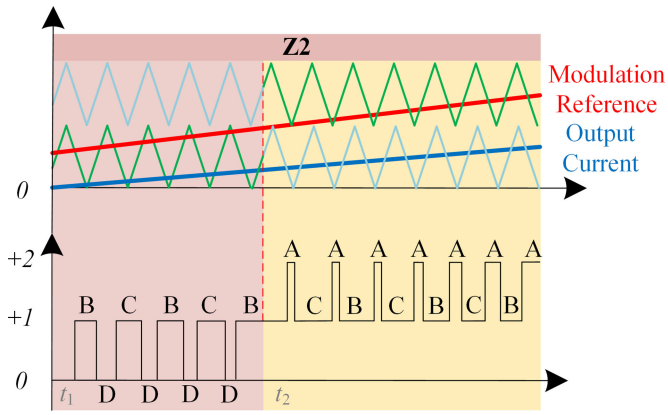

Fig. 8. PWM Modulation in Z2.

charging state B is chosen; when greater than the reference FC voltage, mode C is selected to discharge FC. When outputting the zero voltage level, mode D is chosen. Consequently, the switching state sequence of (B, D, C, D) is achieved.

From t_2 to t_3, the output reference voltage is between +2 and +1. Mode A is required to generate the +2 output level. Similarly, appropriate selection of redundant switching states (B, C) leads to self-balancing of FC. In this way, the sequence of (B, A, C, A) guarantees the FC voltage balancing and inverter output. The modulation in Z2 is shown in Fig. 8.

C. Modulation in Z3 [from t_4 to t_5]

In the capacitive power factor condition, the output current during t_4 to t_5 is positive. Therefore, modes D and G are selected to generate 0 and –1 output, so the circuit rotates in the sequence of (D, G).

D. Modulation in Z4 [From t_5 to t_8]

Similar to Z2, mode E and mode H are selected for zero and –2 output levels. When –1 voltage level is required, redundant

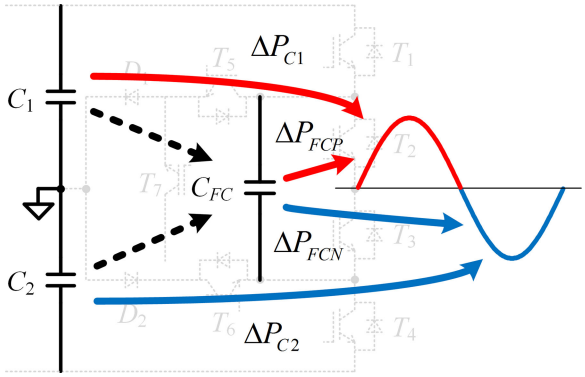

Fig. 9. Relationship of power transmission between dc capacitors, FC, and output side during a whole grid cycle.

switching states (F, G) are employed alternately to keep the FC voltage balanced. Consequently, during t_5 to t_6 and t_7 to t_8, the switching state sequence (F, E, G, E) is achieved; from t_6 to t_7, the switching state sequence (F, H, G, H) is used.

E. DC-Link Capacitor Voltage Balancing

The dc-link capacitor voltage balancing is one problem encountered in single-phase applications, which cannot be solved using a three-phase technique, such as adding zero-sequence voltage. For 5L-ANPC inverters, the output power in a positive grid cycle is provided by the upper side dc capacitor and FC; similarly, the lower dc capacitor and FC are transferring the energy to the output side during the negative grid cycle. If the inverter is controlled to generate the symmetrical output current, then the power relationship can be obtained

$$\Delta P_{C1} + \Delta P_{\mathrm{Fcp}} = \Delta P_{C2} + \Delta P_{\mathrm{Fcn}} \tag{1}$$

where ΔP_{C1}, ΔP_{Fcp} is the energy offered by C_1 and FC in the positive grid cycle, respectively; ΔP_{C2}, ΔP_{Fcn} is the energy from C_2 and FC in the negative grid cycle, respectively. The power transmission relationship is shown in Fig. 9.

It should be noted that the energy provided by FC (ΔP_{Fcp} and ΔP_{Fcn}) also comes from dc-link capacitors (the dashed lines). Based on this, the regulation of dc-link capacitor voltages can be achieved by controlling the FC voltage: if V_{C1} is greater than V_{C2}, then in the positive grid cycle, C_1 can be controlled to transfer more energy to FC and then during the negative grid cycle, FC provides more energy to the output side so that C_2 will output less power. Consequently, the voltage difference between two dc-link capacitors will be decreased. To control the FC voltage, this paper uses the control technique proposed in [27].

V. Flying Capacitor Design

The role of FC in 6S-5L-ANPC inverter is to provide ±1 output voltage levels. In addition to the modulation method, which keeps the FC voltage balanced, selection of FC capacitance which limits its voltage ripple is of equal importance to achieve a stable output voltage level. This section gives the parameter design of FC under unity power factor condition and reactive

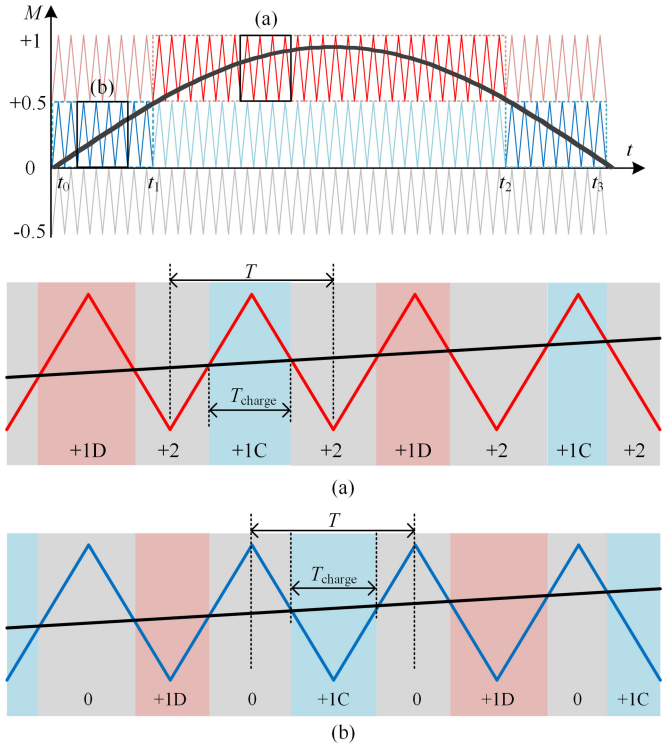

Fig. 10. 6S-5L-ANPC modulation in a positive grid cycle. (a) $M \cdot \sin\theta \geq 0.5$. (b) $M \cdot \sin\theta \leq 0.5$.

power operating condition, and the specific design will also be given.

A. Unity Power Factor Condition

Under the unity power factor condition, the FC design is decided by its voltage ripple. As discussed earlier, the same charging and discharging time during one grid period leads to self-balance of FC. Here, the charging time is used to calculate the FC voltage ripple. The modulation index M is assumed to be greater than 0.5 in consideration of high voltage utilization. Fig. 10 gives the modulation of 6S-5L-ANPC during the positive grid cycle. +2, +1C, and +1D in Fig. 10 represent +2, +1 charging, and +1 discharging output levels, respectively.

From Fig. 10, it is obtained that the charging time of FC (T_{charge}) during one switching cycle (T_S) can be written as

$$\begin{cases} T_{\text{charge}} = \dfrac{2M \cdot \sin\theta}{f_S} & \left(M \cdot \sin\theta \leq \dfrac{1}{2}\right) \\ T_{\text{charge}} = \dfrac{2(1 - M \cdot \sin\theta)}{f_S} & \left(M \cdot \sin\theta \geq \dfrac{1}{2}\right) \end{cases} \tag{2}$$

where f_S is the switching frequency, θ is the reference phase angle. From (2), it is obtained that when $M \cdot \sin\theta \leq 0.5$, the FC charging time function is an increasing function; when $M \cdot \sin\theta \geq 0.5$, it is a monotone decreasing function; and it reaches its peak value, which is T_S when $M \cdot \sin\theta = 0.5$.

During the FC charging time T_{charge}, the FC voltage variation ΔV_{fc} can be calculated using

$$\Delta V_{\text{fc}} = \frac{\Delta Q_{\text{fc}}}{C_{\text{fc}}} = \frac{I_{\text{pk}} \sin\theta \cdot T_{\text{charge}}}{C_{\text{fc}}} \tag{3}$$

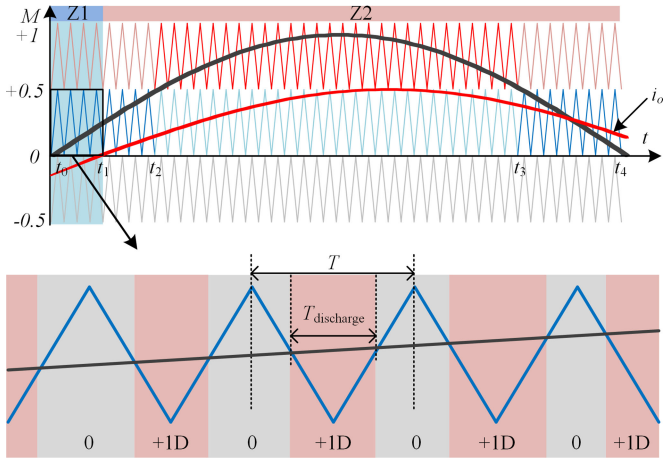

Fig. 11. 6S-5L-ANPC modulation in positive grid cycle under reactive power operating condition.

where I_{pk} is the peak value of the output current. According to (2) and (3), the FC voltage ripple can be written as

$$\begin{cases} \Delta V_{\text{fc}} = \dfrac{2I_{\text{pk}}}{C_{\text{fc}} f_S} \cdot M \cdot \sin^2\theta & \left(M \cdot \sin\theta \leq \dfrac{1}{2}\right) \\ \Delta V_{\text{fc}} = \dfrac{2I_{\text{pk}}}{C_{\text{fc}} f_S} \cdot (-M \cdot \sin^2\theta + \sin\theta) & \left(M \cdot \sin\theta \geq \dfrac{1}{2}\right) \end{cases}. \tag{4}$$

The FC voltage ripple reaches its peak when $\sin\theta = 1/(2M)$. Therefore, the capacitance of FC can be calculated as follows:

$$C_{\text{fc}} = \frac{I_{\text{pk}}}{2\Delta V_{\text{fc}} f_S M}. \tag{5}$$

B. Reactive Power Condition

For 6S-5L-ANPC inverter under reactive power operation, due to the limitation of redundant switching states selection, the FC voltage cannot be regulated in Z1 and Z3 in Fig. 6. According to the analysis earlier, it is observed that FC is continuously discharged in a reactive power region. Thus, the selected FC capacitance value should be large enough to keep the continuous voltage drop within an acceptable range (e.g., 5% of reference FC voltage). As shown in Fig. 6, due to the symmetry, the FC voltage drop in Z1 is the same as Z3, thus the FC voltage drop in Z1 is chosen for calculation. Fig. 11 shows the reactive power modulation of 6S-5L-ANPC inverter during the positive grid cycle, and 0 and +1D in Fig. 11 represent zero and +1 discharging output states.

From Fig. 11, it is observed that in Z1, the output voltage varies between +1 (state B) and 0 (state E). The discharging time of FC ($T_{\text{discharge}}$) during one switching cycle is given by

$$T_{\text{discharge}} = \frac{2M \sin\theta}{f_S}. \tag{6}$$

During each discharging period, the electric charge variation of FC ΔQ_{fc} is calculated according to

$$\Delta Q_{\text{fc}} = i \cdot T_{\text{discharge}} = \frac{2MI_{\text{pk}} \sin^2\theta}{f_S}. \tag{7}$$

To calculate the total electric charge of FC in Z1, the number of switching cycles N in Z1 is required, which is given by

$$N = \frac{\varphi}{2\pi} \cdot \frac{f_S}{f_{\text{Line}}} \tag{8}$$

where f_{Line} represents the line frequency. The relationship of FC capacitance C_{fc}, voltage drop ΔV_{fc}, and electric charge ΔQ_{fc} is then obtained

$$C_{\text{fc}} = \frac{\sum_{n=1}^{N} \Delta Q_{\text{fc}}}{\Delta V_{\text{fc}}} = \frac{2MI_{\text{pk}}}{\Delta V_{\text{fc}} f_S} \cdot \sum_{n=1}^{\frac{\varphi}{2\pi} \cdot \frac{f_S}{f_{\text{Line}}}} \sin^2\left(n \cdot \frac{f_{\text{Line}}}{f_S} \cdot 2\pi\right). \tag{9}$$

For grid-connection application, there will be double line frequency ripple power in dc-link capacitors. With proper dc-capacitance selection, suitable output filter design and control method, the impact of double line frequency ripple power on the output current THD is small. Therefore, the impact of double line frequency ripple power on the FC value calculation can be ignored.

C. Specific Design

As discussed before, the proposed topology is suitable for PV application. This part will give the specific design. For a 1 KVA PV grid-connected system: the grid voltage is 110 V_{RMS}; the dc voltage is 400 V; the switching frequency is 15 KHz; the modulation index is 0.78; the peak-to-peak FC voltage ripple is restricted within 2% of FC voltage. From the FC value calculation (5) in unity power factor condition, the calculated FC capacitance value is 275 μF. And if the system is operating under 0.9 power factor condition, according to (9), a 3.6 V voltage drop is obtained.

Another case is: in 0.9 power factor condition, if the maximum FC voltage drop is 20 V, then based on (9), the calculated FC capacitance is 56 μF. And FC with 56 μF will lead to 10 V peak-to-peak voltage ripple in unity power condition. The simulation section will give the comparison results to show the impact of voltage drop on the output current THD.

VI. Simulation Verification

To verify the effectiveness of the modulation strategy, especially under the reactive power condition as well as the FC capacitance calculation, computer simulation by MATLAB/Simulink has been carried out. The maximum power factor capability of 6S-5L-ANPC inverter is also provided. Based on the specific design in the previous section, the simulation is conducted in two cases: a larger FC value and a smaller FC value. First, to limit the voltage ripple within 2% in a unity power factor condition, the calculated FC value is 275 μF and 310 μF is chosen (part number: 947C311K102CBMS used in experimental prototype). Then, to have 20 V voltage drop in a 0.9 power condition, the calculated FC capacitance is 56 μF. The system parameters are shown in Table V. Each dc-link capacitor is selected to be 2000 μF to limit its voltage ripple within 15 V (= 15 V/ 200 V = 7.5%) according to [23].

TABLE V
System Parameters

Power	1 KVA	Grid Voltage (RMS value)	110 V @ 60 Hz
DC-link Voltage	400 V	Output Filter Inductance	1.6 mH
FC Capacitance	310 μF (947C311K102CBMS)	Power Factor	0.9–1
DC Capacitance	2000 μF each	Switching Frequency	15 KHz

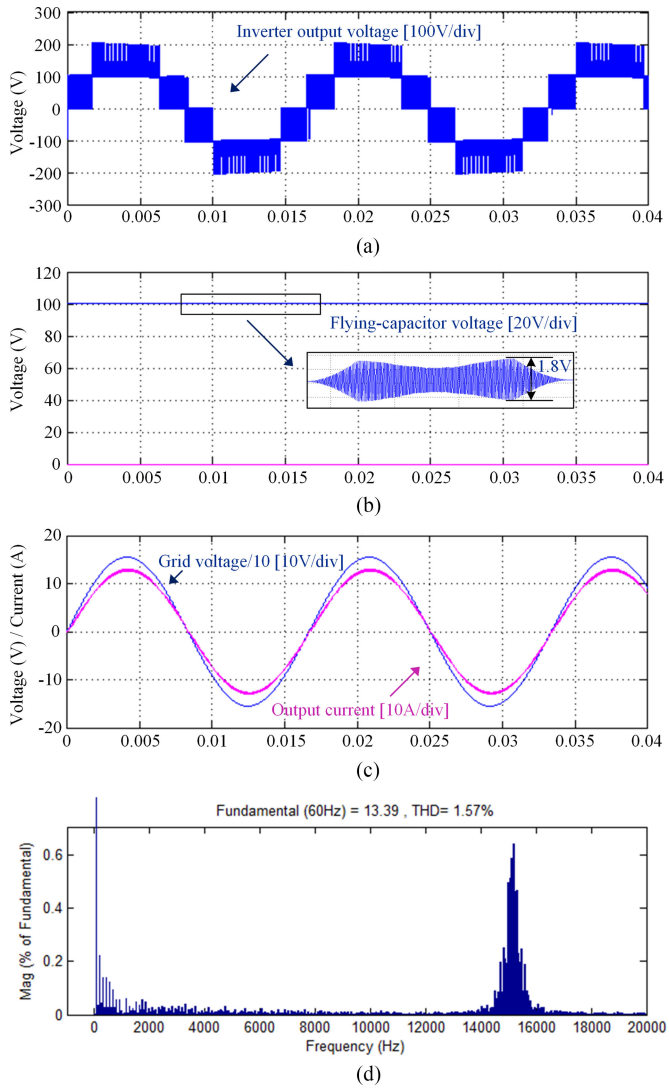

Fig. 12. Simulation results with 310 μF FC value under unity power factor condition. (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

A. Case I: Larger FC Value

First, 310 μF FC value is used for simulation. Fig. 12 gives the simulation results in the unity power factor condition. Fig. 12(a) shows the five-level inverter output. Fig. 12(b) shows the FC voltage. It can be observed that the FC voltage is kept at $V_{\text{dc}}/4$ which is 100 V. A small section of FC voltage waveform in Fig. 12(b) is zoomed to show the voltage ripple. The measured peak-to-peak FC voltage ripple in this case is 1.8 V

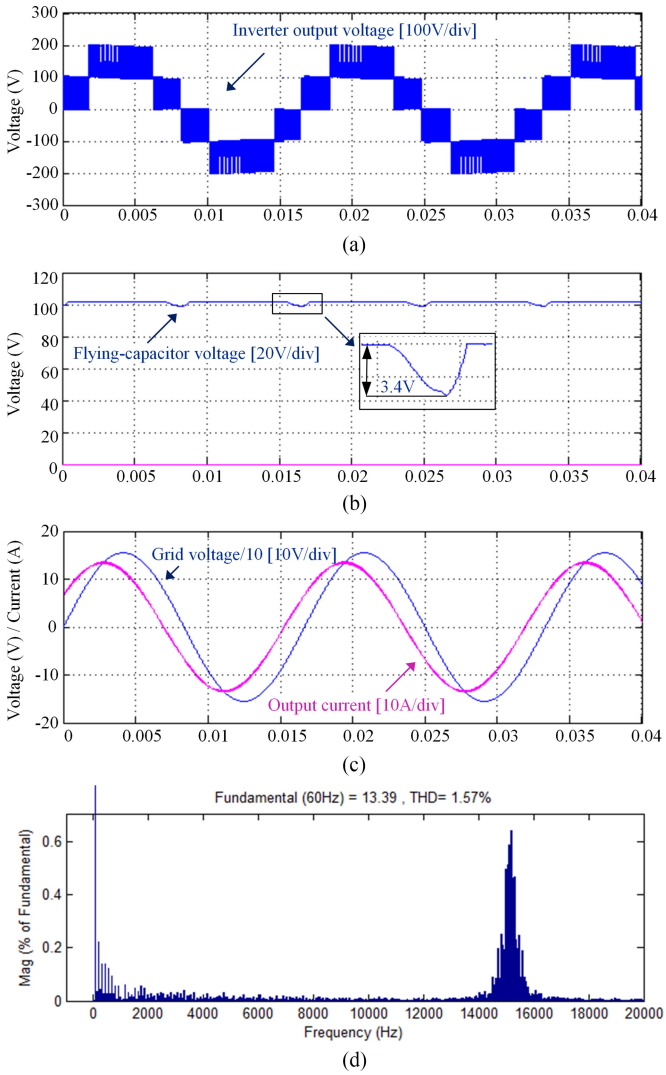

Fig. 13. Simulation results with 310 μF FC value under reactive power operation (PF = 0.9). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

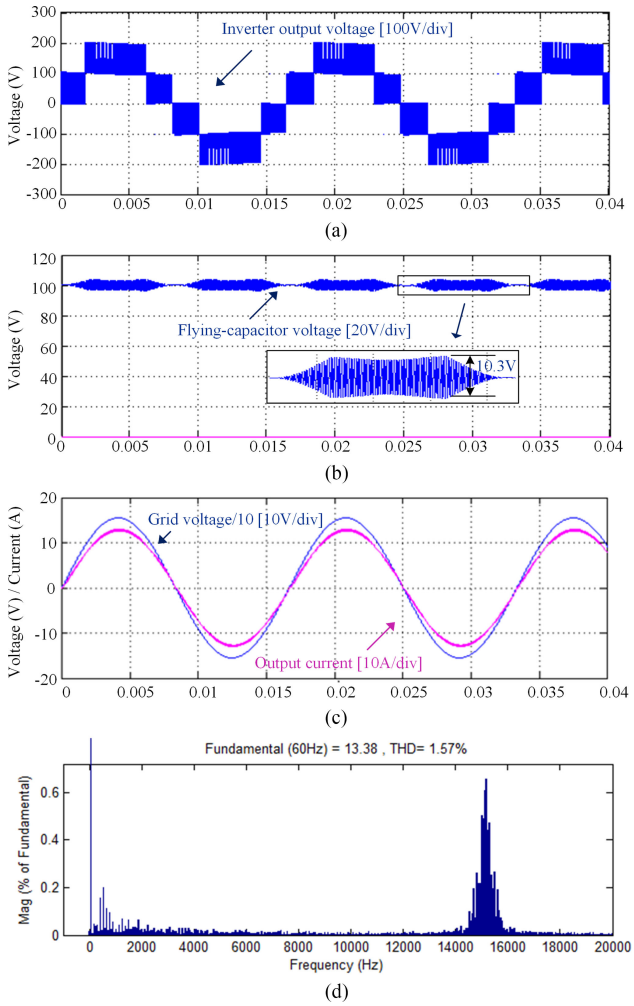

Fig. 14. Simulation results with 56 μF FC value under unity power factor condition. (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

(= 1.8 V/ 100 V = 1.8%). Fig. 12(c) shows the gird voltage and inverter output current. Under unity power factor, the current and voltage are in phase. The output current is sinusoidal wave without distortion. Fig. 12(d) shows the measured output current THD which is 1.57%.

Simulation verification is also carried out under the reactive power condition (PF = 0.9, capacitive). Fig. 13 shows the waveforms of the inverter output voltage, FC voltage, grid voltage, output current, and THD of output current. In Fig. 13(b), it is observed that there is 3.4 V voltage drop in the reactive power region. However, this voltage drop occurs in the region near the zero-crossing point. Since the duty cycles of the output signal in this region are very small, the FC voltage drop has less impact on the output current THD, which is still 1.57%.

B. Case II: Smaller FC Value

To evaluate the impact of FC voltage drop on output harmonics, simulation has also been conducted under smaller FC value condition. The FC capacitance is selected to be 56 μF according to (8) to achieve 20% FC voltage drop. Figs. 14 and 15 show the simulation results in unity power factor and reactive power factor (PF = 0.9) conditions, respectively.

As can be observed in Fig. 14(b), the peak-to-peak FC voltage ripple in the unity power factor condition is increased to 10.3 V. The output current THD is still 1.57%, which is shown in Fig. 14(d). Under a 0.9 PF condition, the FC voltage drop is increased to 20 V, as shown in Fig. 15(b), which verifies the FC design procedures. The output THD in Fig. 15(d) is only increased by 0.03%, which is 1.60%.

C. Low Switching Frequency Operation

From the analysis in Section III, it is concluded that the proposed topology is suitable for high-power application, whose system switching frequency is low (e.g., 2 KHz or lower). Therefore, it is important to evaluate its performance under low switching frequency operation. The switching frequency f_S in this case is selected to be 1.5 KHz. The FC value is 310 μF, and the output filter value is unchanged.

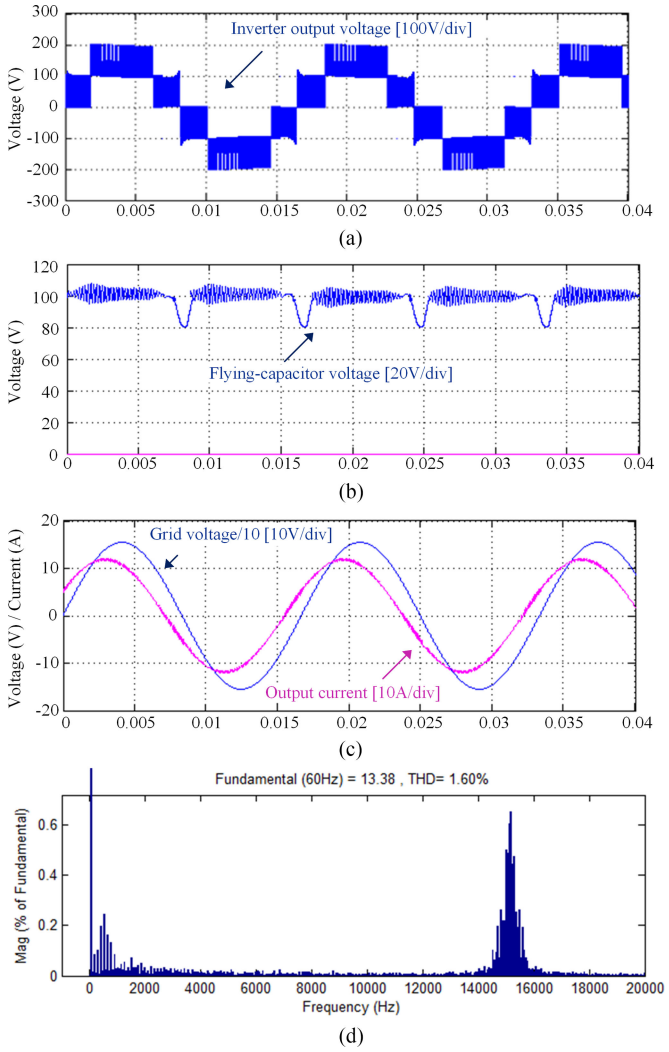

Fig. 15. Simulation results with 56 μF FC value under reactive power operation (PF = 0.9). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

Fig. 16 shows the simulation results when $PF = 1$. As can be observed from Fig. 16(b), the FC voltage ripple is increased to 13 V due to low switching frequency according to (5). Fig. 17 shows the simulation results when PF = 0.9. The measured FC voltage ripple in this case is still 13 V, as shown in Fig. 17(b). Therefore, the FC voltage ripple in both cases (PF = 1 and 0.9) is decided by (5), which is the same as the conventional 5L-ANPC inverter topologies, so the output performance of the proposed topology under a low switching frequency condition is the same as that of conventional 5L-ANPC inverters.

D. Maximum Reactive Power Capability

Although the proposed topology is suitable for unity power factor operation, the functionalities of low-voltage ride-through and the grid support capability are required for the inverters at high-power conversion, even for PV inverters. Therefore, inverters should be capable of injecting some reactive current when the grid presents a voltage sag fault. This part will discuss the maximum power factor capability of the proposed topology.

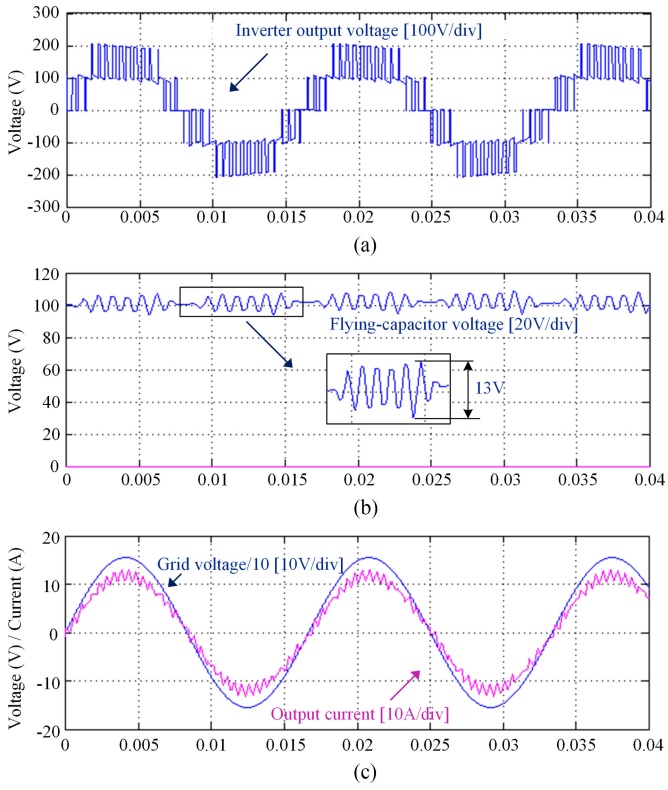

Fig. 16. Simulation results under low switching frequency operation (PF = 1). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current.

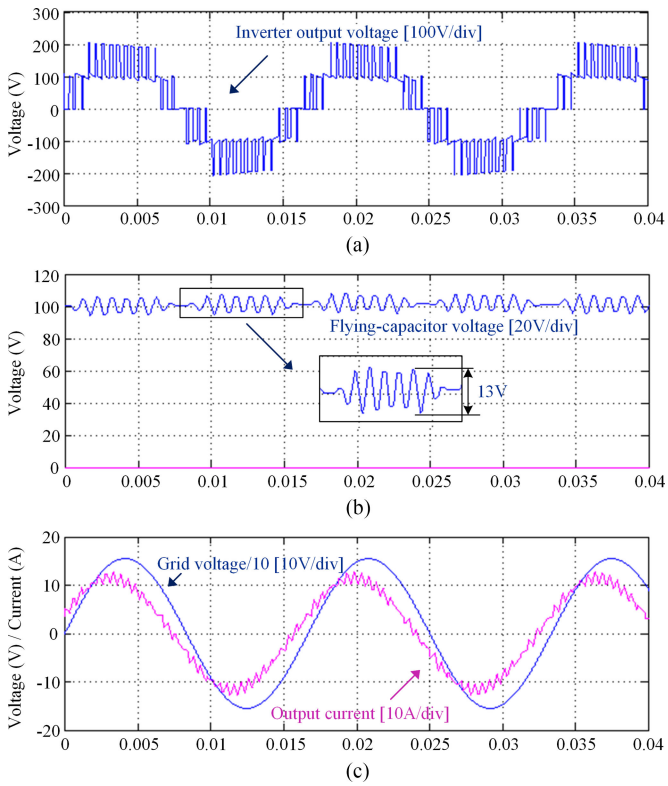

Fig. 17. Simulation results under low switching frequency operation (PF = 0.9). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current.

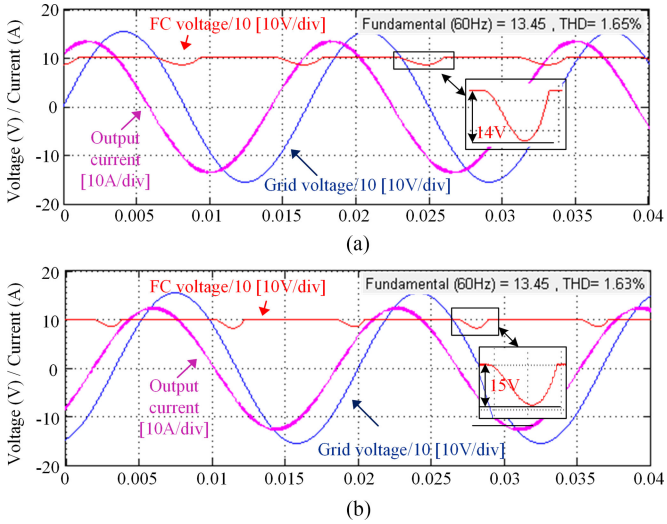

Fig. 18. Simulation results with 15% FC voltage drop using different FC value. (a) FC = 310 μF, PF = 0.6, THD of output current: 1.65%. (b) FC = 56 μF, PF = 0.8, THD of output current: 1.63%.

For 6S-5L-ANPC inverter, there are FC voltage drops under the reactive power condition. This FC voltage drop $\Delta V_{\rm fc}$ will increase the voltage stress of switches T_1 and T_4 by $\Delta V_{\rm fc}$. In addition, even though the output current is compensated by the closed-loop control, high FC voltage drop will cause output current distortion and then limit the maximum power factor capability of the system. Therefore, in consideration of device voltage stress and output performance, the FC voltage drop should be kept within a certain range for a proper system design. In this paper, the FC voltage drop is designed to be less than 15% of the rated FC voltage ($V_{\rm DC}/4$).

From FC capacitance calculation equation under the reactive power condition (9), it is observed that the FC voltage drop value is influenced by FC capacitance, output current value, and power factor. Additionally, with different modulation techniques, the impact of FC voltage drop on the output current performance is also different. Based on the above analysis, it can be concluded that the maximum power factor capability of the system depends on the operation conditions. With the parameters selection in Table V (power level is 1 KVA and FC capacitance is 310 μF), if the FC voltage drop $\Delta V_{\rm fc}$ is 15% of the rated FC voltage which is 15 V, then based on (9) the calculated power factor is around 0.6. Fig. 18(a) shows the simulation waveforms in this case. As can be observed, the output current THD is 1.65%, which is close to that under a unity power factor condition (1.57%). The maximum power factor capability in this case is 0.6.

When the FC value is decreased to 56 μF: based on (9), the calculated power factor is 0.8 to have 15 V FC voltage drop. The simulation result is shown in Fig. 18(b). The measure output current THD is 1.63%, which is also close to the value in the unity power factor condition. For the design requirement in this paper, the maximum power factor capability in this case is 0.8.

VII. Experimental Results

To verify the feasibility and advantages of the proposed topology and its modulation strategy, a 1 KVA single-phase

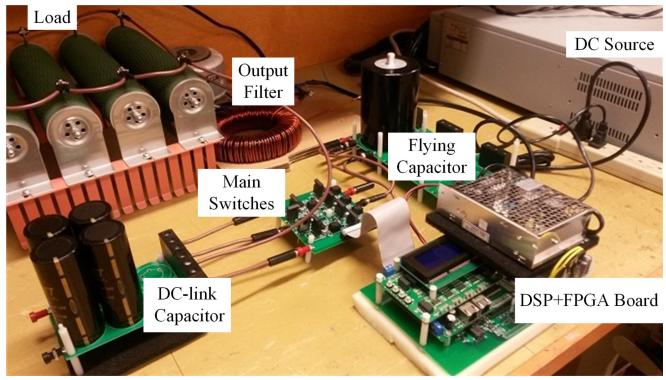

Fig. 19. Experimental prototype.

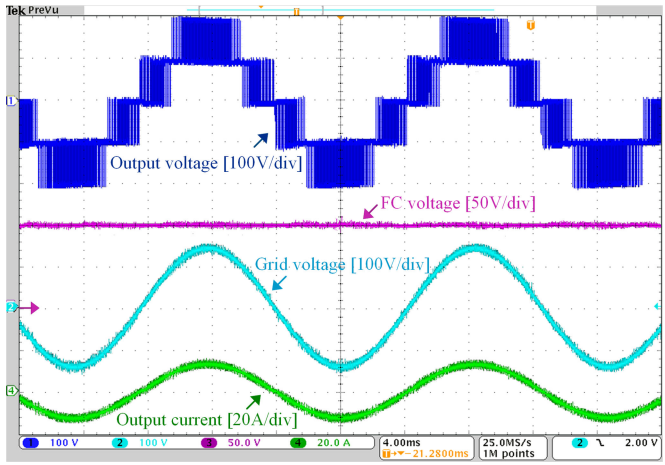

Fig. 20. Experimental results under unity power factor condition: waveforms of inverter output voltage, FC voltage, grid voltage, and output current.

6S-5L-ANPC inverter grid-connected experimental prototype is designed and tested, as shown in Fig. 19. The system includes main circuit, DSP and FPGA control board, DC source, output filter and measurement instruments. The control board employs a combination of the Texas Instruments TMS320F28335 DSP chip and the Altera Cyclone IV EP4CGX22 FPGA card to provide powerful real-time mathematical calculations and control functions. The specifications for experiment are identical to the ones used in the simulation section, which are shown in Table V.

Figs. 20 and 21 show the experimental results under the unity power factor condition. Fig. 20 shows inverter output voltage, FC voltage, grid voltage, and output current: channel 1 is the output bridge voltage; channel 2 is 110 $V_{\rm RMS}$ grid voltage; channel 3 is the FC voltage, which is balanced at 100 V; channel 4 is the output current, which is sinusoidal without distortion and in phase with grid voltage in this case. The measured output current THD is 1.6%. In addition to the FC voltage and ac current waveforms, Fig. 21 also shows the voltages of two dc-link capacitors: channel 1 is lower dc-link capacitor voltage and channel 2 is upper dc-link capacitor voltage. The measured peak-to-peak FC voltage ripple is 2.1 V (= 2.1 V/ 100 V = 2.1%) and dc-link capacitor line-frequency voltage ripple is 12 V (= 12 V/ 200 V = 6%). The balanced FC and dc-link

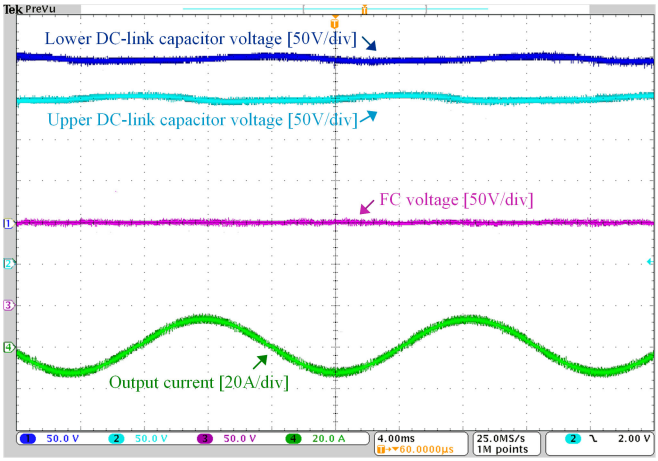

Fig. 21. Experimental results under unity power factor condition: waveforms of lower dc-link capacitor voltage, upper dc-link capacitor voltage, FC voltage, and output current.

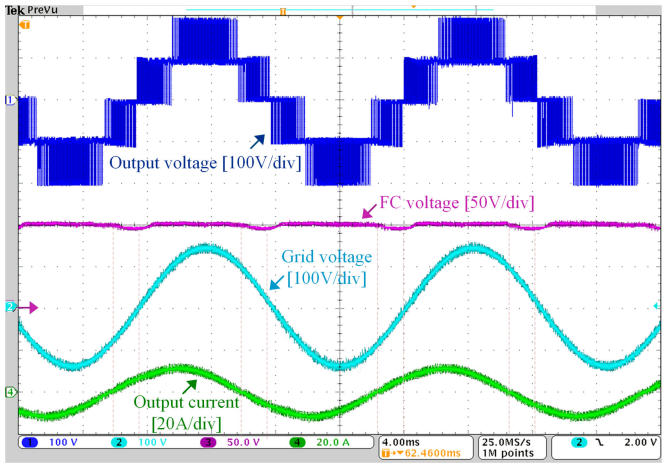

Fig. 22. Experimental results under reactive power operation (PF = 0.9, capacitive): waveforms of inverter bridge voltage, FC voltage, grid voltage, and output current.

capacitors voltages verify the modulation method in an active power condition.

The reactive power operation mode is also tested. The power factor is selected to be 0.9 (capacitive). Figs. 22 and 23 show the experimental results.

In Fig. 22, channel 1 shows the five-step waveform of the bridge voltage. Channel 3 shows the FC voltage waveform. As can be observed, the continuous FC voltage drop is 4 V ($= 4$ V/ 100 $V = 4\%$). The grid voltage in channel 2 leads the inverter output current in channel 4 by 25° because of 0.9 system power factor. In this situation, the inverter still produces good quality current waveform without distortion. The measured THD value of the output current is still 1.6%.

Fig. 23 shows two DC-link capacitors voltages, FC voltage, and output current. The dc-link capacitors voltages waveforms in this situation are almost the same as the one under the active power condition. The measured peak-to-peak dc-link capacitor ripple voltage is 11.4 V ($= 11.4$ V/ 200 $V = 5.7\%$).

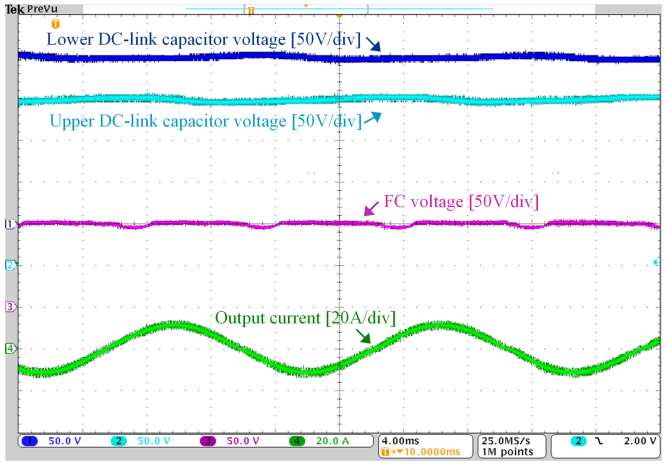

Fig. 23. Experimental results under reactive power condition ($PF = 0.9$, capacitive): waveforms of lower dc-link capacitor voltage, upper dc-link capacitor voltage, FC voltage, and output current.

VIII. Conclusion

In this paper, a novel 6S-5L-ANPC inverter topology has been proposed. As compared with the conventional 5L-ANPC inverter, it requires only six switches for a single phase, a reduction from eight switches. The operating principles and switching states are presented. The results of comparison between 6S-5L-ANPC and the conventional 5L-ANPC topologies show that the 6S-5L-ANPC topology has lower conduction loss and thus higher efficiency in a high-power condition. The specific modulation strategy of 6S-5L-ANPC inverter under reactive power operation has been proposed. Issues related to the dc-link capacitors and FC voltages balancing and the maximum reactive power capability are discussed. The equations to calculate the FC capacitance value in active and reactive power conditions are provided. Computer simulation and experimental prototype based on a single-phase 1 KVA prototype have been carried out in both active and reactive power conditions to demonstrate the reliability of the proposed topology and modulation method.

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